

REMARKS

The Applicant sincerely appreciates the thorough examination of the present application as evidenced by the Office Action of March 8, 2005. In particular, the Applicant appreciates the Examiner's indication that Claims 2-9, 14-20, 27-29, 32, 35-37, 40, and 42-49 would be allowable if rewritten in independent form. In response, the Applicant has amended Claim 1 to include all recitations of Claim 2 (indicated allowable); canceled Claim 2; amended Claims 3, 4, and 8 to depend from Claim 1; amended Claim 13 to include all recitations of Claim 14 (indicated allowable); canceled Claim 14; amended Claims 15, 16, and 20 to depend from Claim 13; amended Claims 7 and 19 to more clearly define the claimed invention; and canceled Claims 25-40 and 50-55. In addition, Claim 41 has been amended to correct minor informalities noted therein without affecting scope of the claim. Claims have been canceled and/or amended herein to advance prosecution of the present application without prejudice to the Applicant's right to pursue these claims in a continuing and/or divisional application.

Accordingly, Claims 1, 3-13, and 15-24 have been placed in a condition indicated allowable by the Examiner. In the following remarks, the Applicant will show that independent Claim 41 is patentable over Moyal and that dependent Claims 42-49 are patentable at least as per the patentability of Claim 41 from which they depend. Accordingly, dependent Claims 42-49 (all indicated allowable) have not been rewritten in independent form. All pending claims are, thus, patentable over the cited art, and a Notice of Allowance is respectfully requested in due course.

Claim 41 Is Patentable Over Moyal

Claim 41 has been rejected as being anticipated by U.S. Patent No. 6,329,840 to Moyal ("Moyal"). Claim 41, however, is patentable over Moyal for at least the reasons discussed below. In particular, Claim 41 recites an output buffer circuit including:

a pull-up transistor which pulls up an output terminal in response to a pull-up control signal;

a pull-down transistor which pulls down the output terminal in response to a pull-down control signal;

a NAND gate which receives at least one control signal and data and generates the pull-up control signal; and

a NOR gate which receives an inverted signal of the control signal and the data and generates the pull-down control signal,

wherein a number of PMOS transistors present along a path of a first supply voltage to an output terminal of the NAND gate is equivalent to a number of PMOS transistors present along a path of the first supply voltage to an output terminal of the NOR gate, and a number of NMOS transistors present along a path of a second supply voltage to an output terminal of the NAND gate is equivalent to a number of NMOS transistors present along a path of the second supply voltage to an output terminal of the NOR gate.

The Applicant respectfully submits that Moyal fails to teach or suggest the recitations of Claim 41. More particularly, Moyal fails to teach or suggest a output buffer circuit including a NAND gate that generates a pull-up control signal for a pull-up transistor and/or a NOR gate that generates a pull-down signal for a pull-down transistor, as recited in Claim 41. In support of the rejection, the Office Action states that Moyal shows:

a first logic gate (128a) configured to generate the pull-up control signal...;

a second logic gate (128b) configured to generate the pull-down control signal....

Office Action pages 2-3. The Office Action further states that Moyal shows:

A buffer circuit ... wherein the first logic gate comprises a NAND gate (M1-M6) and wherein the second logic gate comprises a NOR gate (M9-M14).

Office Action, page 3.

In response, the circuit 128a including transistors M1-M6 of Moyal configured to generate the pull-up control signal as set forth in the Office Action is not a NAND gate.

Moreover, the circuit 128b including transistors M9-M14 of Moyal configured to generate the pull-down control signal as set forth in the Office Action is not a NOR gate.

With respect to the circuit including transistors M1-M6 of Figure 7 of Moyal, the Tri-State+ input to gates of transistors M1 and M6 may be labeled T+, the data input to gates of transistors M2 and M3 may be labeled A-, and the output of the circuit (including transistors M1-M6) may be labeled X (*i.e.*, at the node between transistors M5 and M6). The functionality of

the circuit including transistors M1-M6 of Moyal can thus be expressed using the truth table below:

| T+ | A- | - | X |
|----|----|---|---|
| 0 | 0 | - | 1 |
| 0 | 1 | - | 0 |
| 1 | 0 | - | 0 |
| 1 | 1 | - | 0 |

The circuit including transistors M1-M6 of Moyal, thus, provides the functionality of a NOR gate. (The truth table for a NOR gate is provided in the document entitled "Understanding Logic Gates – TRUTH TABLE FOR THE 'NOR' GATE" submitted with the Information Disclosure Statement filed concurrently herewith.) Accordingly, Moyal fails to teach or suggest a first logic gate comprising a NAND gate 128a (including transistors M1-M6) that are configured to generate a pull-up control signal as set forth in the Office Action.

With respect to the circuit including transistors M9-M14 of Figure 7 of Moyal, the Tri-State- input to gates of transistors M12 and M13 may be labeled T-, the data input to gates of transistors M10 and M11 may be labeled A-, and the output of the circuit (including transistors M1-M6) may be labeled Y (*i.e.*, at the node between transistors M13 and M14). The functionality of the circuit including transistors M9-M14 of Moyal can thus be expressed using the truth table below:

| T- | A- | - | Y |
|----|----|---|---|
| 0 | 0 | - | 1 |
| 0 | 1 | - | 1 |
| 1 | 0 | - | 1 |
| 1 | 1 | - | 0 |

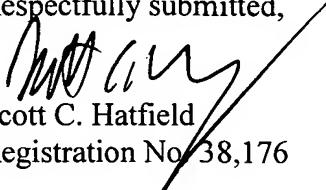
The circuit including transistors M9-M14 of Moyal, thus, provides the functionality of a NAND gate. (The truth table for a NAND gate is provided in the document entitled "Understanding Logic Gates – TRUTH TABLE FOR THE 'NAND' GATE" submitted with the Information Disclosure Statement filed concurrently herewith.) Accordingly, Moyal fails to teach or suggest a second logic gate comprising a NOR gate 128b (including transistors M9-M14) that are configured to generate a pull-up control signal as set forth in the Office Action.

For at least the reasons discussed above, the Applicant respectfully submits that Moyal fails to teach or suggest the output buffer circuit of Claim 41, and that Claim 41 is thus patentable. The Applicant further submits that dependent Claims 42-49 are patentable at least as per the patentability of Claim 41 from which they depend. Dependent Claims 42-49 are also independently patentable as set forth on page 6 of the Office Action.

CONCLUSION

Accordingly, the Applicant submits that all pending claims in the present application are in condition for allowance, and a Notice of Allowance is respectfully requested in due course. The Examiner is encouraged to contact the undersigned attorney by telephone should any additional issues need to be addressed.

Respectfully submitted,


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